1. (Amended) A ferroelectric memory, comprising:

an insulation film having a hollow at a top surface;

a laminated body obtained by laminating a plurality of layers on said top surface and etching a region of said plurality of layers corresponding to a region other than said hollow, wherein said laminated body includes a lower electrode layer, a ferroelectric layer formed on said lower electrode layer and an upper electrode layer formed on said ferroelectric layer.

REMARKS

The Office Action mailed May 9, 2001 and the references cited therein have been carefully considered. The specification and Claim 1 have been amended in a sincere effort to further clarify the subject matter Applicant regards as the invention. In addition, Claims 6-14 have been cancelled without prejudice to their incorporation in a divisional application to be filed.

No new matter has been added to the specification or claims as amended. Support for this Amendment is found generally within the specification, claims, and drawings, as filed. As a result of this Amendment taken together with the remarks set forth below, it is respectfully submitted that pending Claims 1-5 are now before the Examiner in condition for favorable consideration and allowance.

In the Office Action, Claims 1, 2, and 4 have been rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,614,438 to Evans, et al. (*Evans*). Specifically, the Examiner contends that *Evans* discloses (at column 2, line 62 to column 4, line 36) a ferroelectric memory device having the elements recited in Claim 2.

and the lower electrode 42, as shown in Figure 4. Regarding Claim 4, the Examiner contends

that *Evans* discloses a lower electrode formed on the surface of the same material as that of the lower electrode (at column 3, lines 34-38).

In addition, Claims 3 and 5 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over *Evans* in view of U.S. Patent No. 6,078,093 to Lee (*Lee*). Regarding Claim 3, the Examiner concedes that *Evans* does not disclose that the lower electrode includes two portions, but contends that *Lee* teaches that the first lower electrode portion formed in a hollow is a barrier layer that prevents the formation of the interface oxide film. Thus, the Examiner contends that it would have been obvious at the time the invention was made to have two lower electrode portions to prevent the formation of oxide in the interface.

Regarding Claim 5, the Examiner contends that *Evans* does not disclose that the lower electrode and the insulation film are planarized flush with each other, but that *Evans*, as modified by *Lee*, discloses the first and second lower electrode portions. The Examiner further contends that *Lee* discloses that the layers are polished and planarized to expose an insulation layer 28 (at column 6, lines 30-36).

The subject invention is directed to a ferroelectric memory, which includes an insulation film and a laminated body. The insulation film has a hollow and a top surface. The laminated body is obtained by laminating a plurality of layers on the top surface and etching a region of the plurality of layers corresponding to a region other than the hollow. The laminated body includes a lower electrode layer, a ferroelectric layer formed on the lower electrode layer, and an upper electrode layer formed on the ferroelectric layer, as now defined by amended Claim 1.

As recited in amended Claim 1, the plurality of layers including the lower electrode layer, the ferroelectric layer, and the upper electrode layer are laminated on the top surface of

layer is formed in the hollow, the period of time required for the etching process is shortened, which substantially prevents the deterioration of ferroelectric characteristics, as disclosed at page 1, line 25 to page 2, line 9; page 7, lines 3-11; page 7, line 23 to page 8, line 4; and page 9, lines 1-20 of the specification.

Evans relates to a method for making small electrodes for use with ferroelectric-based capacitors. Problems associated with the deposition and etching of a lanthanum strontium cobalt oxide (LSCO) layer during the generation of platinum features on a surface of a substrate are allegedly overcome by utilizing low-temperature sputtering of the LSCO layer.

The *Evans* method includes depositing a layer of titanium on a substrate and then masking the titanium layer and regions outside the area to be covered by the electrode. The exposed regions of the titanium layer are then etched. A new layer of titanium is deposited followed by a layer of platinum. The LSCO material is then sputtered onto the platinum layer at room temperature. The masking material is removed leaving the platinum electrode bonded to the substrate by the newly deposited titanium layer. The resulting structure is then crystallized by heating it to a high temperature.

However, *Evans* does not teach or suggest a hollow being formed on a top surface of an insulation film, as now defined by amended Claim 1. Rather, *Evans* describes an additional titanium oxide (TiO_2) layer deposited on the SiO_2 layer to prevent contact between materials in the electrode stack and the underlying SiO_2 layer, as described at column 3, lines 3-13.

The Examiner contends that reference numeral 45 in *Evans* is a lower electrode, reference numeral 46 is a ferroelectric, and reference numeral 54 is an upper electrode. However, reference numeral 45 refers to a titanium base layer, reference numeral 46 refers to

could not be considered the ferroelectric and the upper electrode layers, respectively. Further, the laminated body formed by the titanium base layer, the platinum electrode layer, and the LSCO layer is actually an ohmic contact, which is entirely different from the ferroelectric memory recited in Claim 1. Thus, *Evans* fails to teach or suggest the ferroelectric memory, as now defined by amended Claim 1.

Lee relates to a capacitor structure with a high dielectric constant suitable for fabrication on semiconductor devices. The capacitor includes a semiconductor substrate having an impurity diffusion region, an insulating layer formed on the semiconductor substrate having a contact hole in the impurity diffusion region, and a first lower electrode formed on the insulating film along an upper edge of the contact hole.

The capacitor also includes a second lower electrode formed on a surface of the substrate exposed through the contact hole, a dielectric layer formed on the first and second lower electrodes, and an upper electrode formed on the dielectric layer. However, *Lee* does not teach or suggest a ferroelectric formed on a lower electrode, as now defined by amended Claim 1.

Lee also describes a lower electrode, a dielectric layer formed on the lower electrode, and an upper electrode formed on the dielectric layer. However, according to *Lee*, neither the dielectric layer nor the upper electrode formed on the lower electrode is subjected to the etching process. Therefore, the dielectric layer and the upper electrode are formed not only on a region corresponding to the hollow, but also on regions other than the hollow. Thus, the structure of the lower electrode, the dielectric layer, and the upper electrode is substantially different from that of the laminated body, as now defined by Claim 1.

Since *Evans* fails to teach or suggest a laminated body in which a ferroelectric or

[illegible]

if both references are combined, the result will not have a structure even remotely similar to that of the present invention. Therefore, the structure recited in Claim 1 is neither taught nor suggested by the combination of *Evans* and *Lee*.

Applicant respectfully notes that in order to support a claim of *prima facie* anticipation, a single reference must teach or enable each of the claimed elements as arranged in the claim interpreted by one of ordinary skill in the art. Further, in order to support a claim of *prima facie* obviousness, the cited references must teach or suggest each and every element of the invention, and there must be a motivation in the references or the prior art to combine the references as suggested.

However, none of the art of record teaches or suggests, either alone or in combination a ferroelectric memory, which includes an insulation film and a laminated body obtained by laminating a plurality of layers on a top surface of an insulation film and etching a region of the plurality of layers corresponding to a region other than the hollow. The laminated body includes a lower electrode layer, a ferroelectric layer formed on the lower electrode layer, and an upper electrode layer formed on the ferroelectric layer, as now defined by amended Claim 1.

Applicant respectfully submits that Claims 2-5, which depend from Claim 1 are patentable over the art of record by virtue of their dependency from Claim 1, which is believed patentable for the reasons set forth above. Further, Applicant submits that Claims 2-5 define additional patentable subject matter in their own right. Therefore, it is respectfully requested that the rejection of Claims 1, 2, and 4 under 35 U.S.C. § 102(b) and the rejection of Claims 3 and 5 under 35 U.S.C. § 103(a) be reconsidered and withdrawn.

In view of the foregoing Amendment and remarks, entry of the amendments to the specification and Claim 1, favorable consideration of Claim 1 as amended, favorable reconsideration of Claims 2-5, and allowance of pending Claims 1-5 are respectfully and earnestly solicited.

Respectfully submitted,

Rod S. Turner

Rod S. Turner
Registration No.: 38,639
Attorney for Applicant

HOFFMANN & BARON, LLP
6900 Jericho Turnpike
Syosset, New York 11791
(516) 822-3550
RST/jp

139034_1.DOC

VERSION OF AMENDMENT WITH MARKS TO SHOW CHANGES MADE

IN THE SPECIFICATION:

At page 1, replace the paragraph beginning at line 25 and ending at page 2, line 9 with the following:

In the prior art, however, a conductive film 5a, a ferroelectric film 4a and a conductive film 3a are formed to a thickness to provide an upper electrode 5, a ferroelectric film 4 and a lower electrode 3, so that dry etching is then conducted throughout a total film thickness in order to remove unwanted portions of these films[,]. Thus, the prior art has required a much greater etch amount and hence a [long] longer etch time. This results in [long-time] longer exposure of the ferroelectric film 4 to the plasma atmosphere during a dry etch process. The plasma however has effects upon the ferroelectric 4 [to] that lower its switching charge amount (Qsw). Thus, there has been a fear of causing such [problem] problems as worsening the symmetry in hysteresis and deteriorating the characteristics of coerciveness and fatigue.

At page 6, replace the paragraph beginning at line 2 with the following:

A method for manufacturing a ferroelectric memory 10 will now be explained concretely with reference to Figure 2 and Figure 3. First, not-shown silicon (Si) substrate is prepared, to form thereon by a CVD technique a first insulation film 12 of silicate glass containing phosphorus (PSG), silicate glass containing boron/phosphorus (BPSG) or the like. Subsequently, as shown in Figure 2(A) the first insulation film 12 is masked by a patterned resist 24 to form a hollow 14 by an RIE (reactive ion etching) technique as anisotropic dry etching. Then, as [shwon] shown in Figure 2(B), a first conductive film 26 as a gel dry film is formed by a sol-gel technique on a surface of the first insulation film 12 including an inside

This solution is applied onto a surface of the first insulation film 12 by a spin coating technique, and then dried into a gel dry film. In an application process using a spin coating technique, the precursor solution dripped on the surface of the first insulation film is splashed away due to a centrifugal force. However, the precursor solution existing inside the hollow 14 will not readily <u>be</u> splashed away. This provides the first conductive film 26 with a film thickness that is greater [at] inside the hollow 14 than the other portion, as shown in Figure 2(B).

<u>At page 7, replace the paragraph beginning at line 23 with the following:</u>

According to the present embodiment, a hollow 14 was formed in the top surface of the insulation film 12 so that a lower electrode 16 can be formed inside the hollow 14 by the sol-gel technique including a spin-coating application process. At stated before, it is therefore possible to decrease an etch time to provide a lower electrode 16. This in turn reduces the time for which the film 28 for providing a ferroelectric 18 is exposed to a dry-etching plasma atmosphere. Thus, the ferroelectric 18 can be prevented from being deteriorated in characteristics by the [affection] <u>effects</u> of a plasma.

<u>At page 10, replace the paragraph beginning at line 6 with the following:</u>

Meanwhile, as shown in Figure 10, a first electrode portion 16a may be formed at a corner of the hollow 14 by a process including spin coating (e.g. sol-gel technique) so that a second electrode portion 16b can be formed to provide a lower electrode 16. In this case, if the second electrode portion 16b is formed by a process including a spin coat technique (e.g. sol-gel technique), it is possible to [decreases] <u>decease</u> an amount of depression to be caused in a top surface center there of upon baking the lower electrode 16. Meanwhile, if the second electrode portion 16b, or first conductive film 26b, is formed by sputtering, the variation in crystalline orientation is reduced in a top surface of the lower electrode 16, as shown in

over the entire bottom surface of the hollow 14 as shown in Figure 12, the second electrode portion 16b can be made thin in thickness by a corresponding amount to the film thickness of the first electrode portion 16a. This [reduce] reduces the amount of etching to be [conductede] conducted in the etching process.

IN THE CLAIMS:

Please cancel Claims 6-14 without prejudice to incorporating the same in a divisional application to be filed.

Please amend Claim 1 by rewriting the same as follows:

1. (Amended) A ferroelectric memory, comprising:

an insulation film having a hollow at a top surface;

[a hollow formed in a top surface of said insulation film;]

a laminated body obtained by laminating a plurality of layers on said top surface and etching a region of said plurality of layers corresponding to a region other than said hollow, wherein said laminated body includes a lower electrode layer [formed in said hollow;], a ferroelectric layer formed on said lower electrode layer [;] and an upper electrode layer formed on said ferroelectric layer.